

METHOD AND APPARATUS FOR DATA
COMPRESSION IN MEMORY DEVICES

ABSTRACT OF THE DISCLOSURE

A test circuit for a memory device having a pair of arrays each of which includes a plurality of memory cells arranged in rows and columns. A pair of complementary digit lines is provided for each column of each array. The digit lines are selectively coupled to a pair of I/O lines for each array which are, in turn, coupled to a pair of complementary data lines. The data lines are coupled to respective inputs of a DC sense amplifier, one of which is provided for each array. A multiplexer connects the pair of I/O lines for either one of the arrays to the data lines in a normal operating mode. Thus, in the normal operating mode, data are selectively coupled to the inputs of the DC sense amplifier from the complementary digit lines for an addressed column. In a test mode, the multiplexer connects the I/O lines for both arrays to the data lines to compress the data from the two arrays. Combinatorial logic then determines if both of the data lines have the same logical value, indicating disagreement between the data from the memory arrays that may indicate the presence of a defective memory cell in one or the other array. Thus, in the test mode, data are simultaneously coupled to the inputs of the DC sense amplifier from respective digit lines coupled to two different memory cells, thereby increasing the rate at which background data that has been written to the arrays can be read from the arrays.

0996413.092504
T05260.ET49660